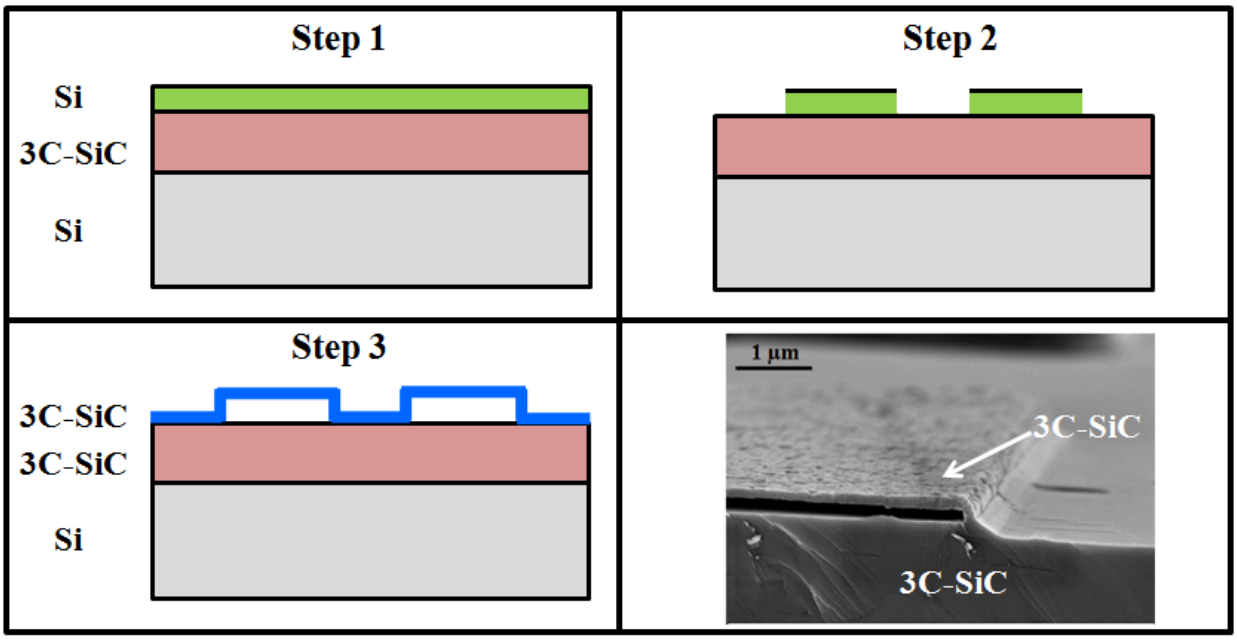
Implementation of an insulating layer between two cubic silicon carbide layers for MEMS applications

Context:

The cubic polytype of silicon carbide (3C-SiC) appears as a potential alternative to replace Si in many applications due to its excellent mechanical and electrical properties. Furthermore, the 3C-SiC can be heteroepitaxied on low-cost and large-area Si substrates which render the cubic polytype distinguished compared to the hexagonal SiC phases. Recently, our group was investigating the possibility to achieve 3C-SiC/Si/3C-SiC heterostructure on Si substrate which can pave the road towards original and new micro-electro-mechanical-systems (MEMS) [1,2].



However, the implementation of an insulating layer to separate the two 3C-SiC layers is required for some applications. Therefore, we aim to investigate the implementation of an insulating layer (silicon nitride, silicon dioxide) which is able to stand in temperature for the subsequent 3C-SiC growth which is performed at around 1300ºC.

Subject:

The internship student will be responsible of the optimization of the insulating layer growth by means of chemical vapor deposition (CVD). Then performing the etching of this layer in the desired shape using clean room facilities. After that, the influence of thermal annealing tests will be investigated and the effect of such treatments on the surface morphology will be assessed.

Techniques: CVD, SEM, AFM, XRD, photolitography, reactive ion etching.

Required profile: Master II student in microelectronics with solid background in semiconductor physics. The candidate have to be autonomous with the ability to work in group. Candidates with experience in clean room are encouraged to apply. Interested candidates are kindly required to send a CV and a cover letter to the email addresses given below.

Duration and Location: 6 months starting in March 2016 at GREMAN laboratory, University François Rabelais, Tours.

Contact: Dr. Jean François Michaud
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Rami Khazaka, PhD student
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Related publications:

[1] J.F. Michaud, M. Portail, T. Chassagne, M. Zielinski, D. Alquier, Original 3C-SiC micro-structure on a 3C-SiC pseudo-substrate, Microelectronic Engineering 105 (2013) 65-67.

[2] R. Khazaka, E. Bahette, M. Portail, D. Alquier, J.F. Michaud, Toward high-quality 3C–SiC membrane on a 3C–SiC pseudo-substrate, Materials Letters 160 (2015) 28-30.